PATH PLANNING WITH LOIHI

Neuromorphic Computing Lab | Intel Labs

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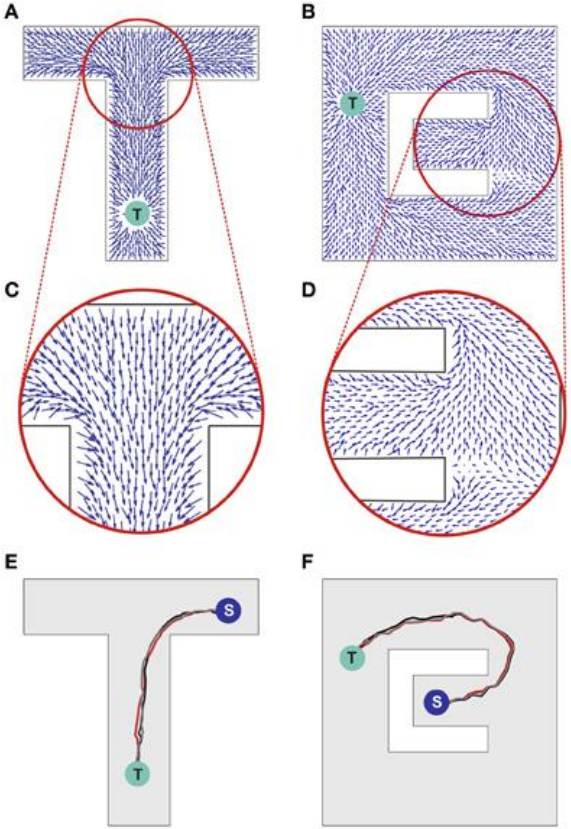
Path Planning with Spike Wavefronts



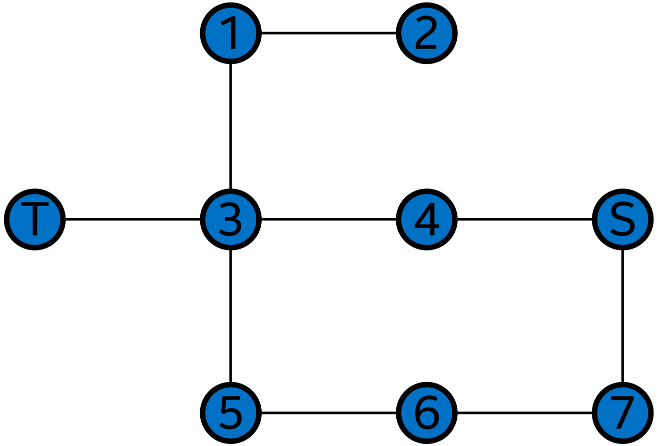
Hopfield[1] modeled how the brain might solve spatial navigation problems using parallel exploration of alternative routes through propagating waves of spiking activity

[1] Ponulak F., Hopfield J.J. Rapid, parallel path planning by propagating wavefronts of spiking neural activity. Front. Comput. Neurosci. 2013. V. 7. Article № e98.

Optimized (exact) spiking graph search algorithm (1)

Initial state:

- All edges have bidirectional synaptic connections



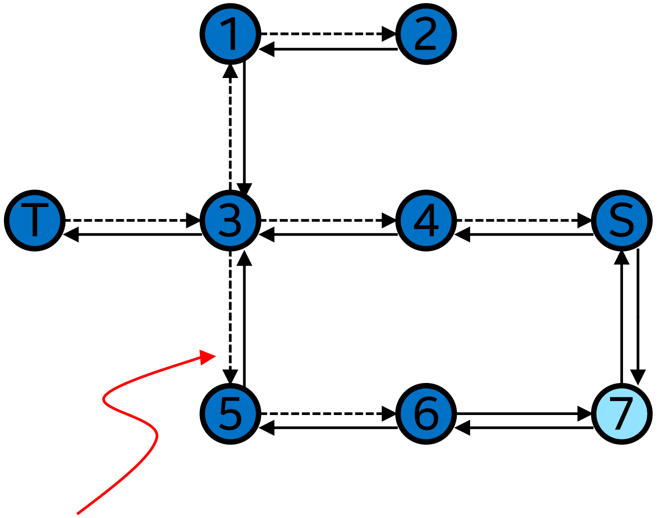
Optimized (exact) spiking graph search algorithm (2)

Phase 1 wavefront propagation:

- Spike wavefront propagates from Target (T) to Source (S)
- **First arriving spike** at each node causes **input weight to be zeroed**

End state:

- Zeroed edges form a spanning tree over all nodes between T and S within diam(S,T).
- Non-zeroed edges point in direction of shortest path back to T.



Wavefront arrives first from 3->5, so weight is zeroed

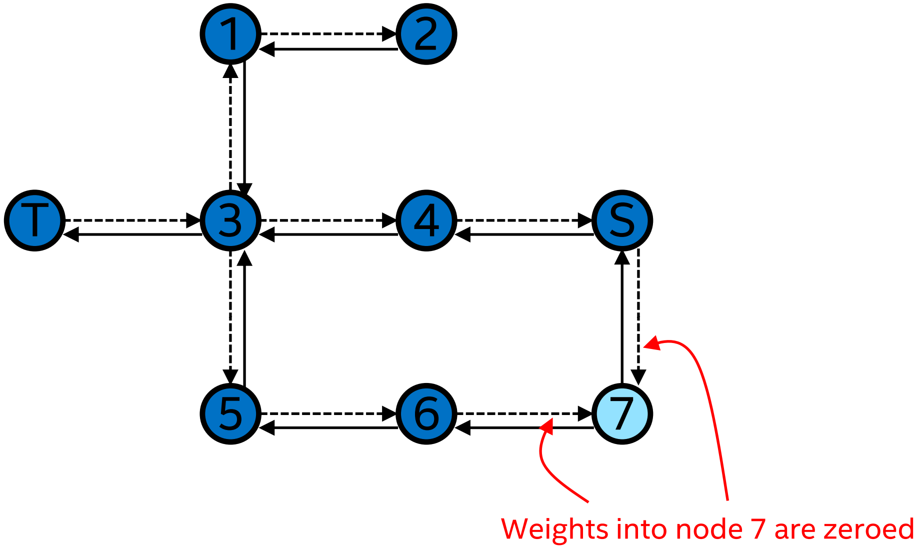
Optimized (exact) spiking graph search algorithm (3)

Phase 1 cleanup:

- After S fires, **weights into unfired nodes are zeroed**

End state:

- S only has one nonzero fanout edge

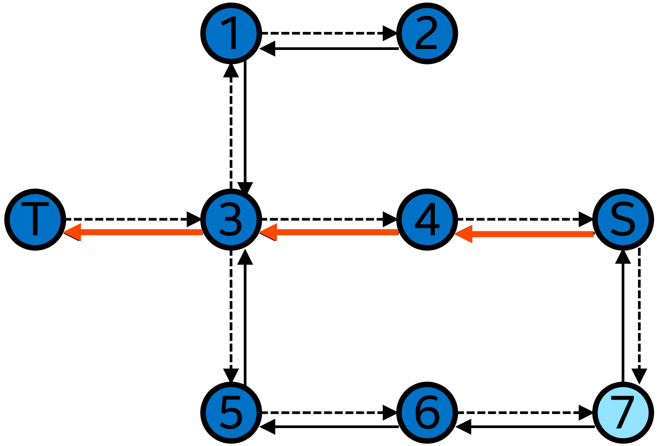


Optimized (exact) spiking graph search algorithm (4)

Phase 2:

- Trace path with non-zero weights from S->T to read out shortest path

(∃ only *one path* S->T due to graph's spanning tree structure after phase 1)



Tutorial: Path Planning

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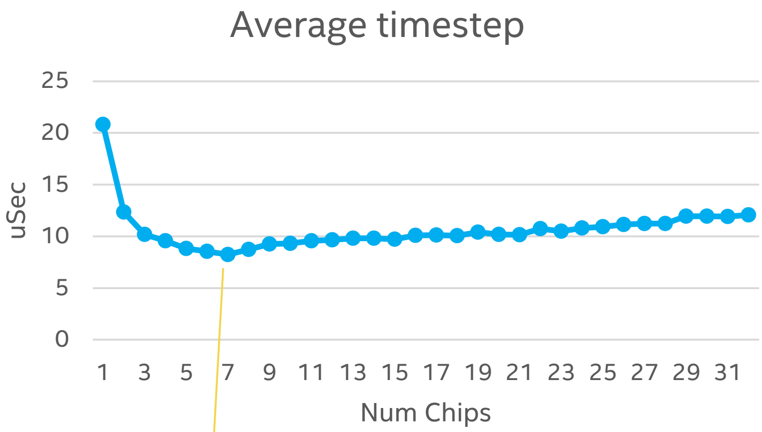
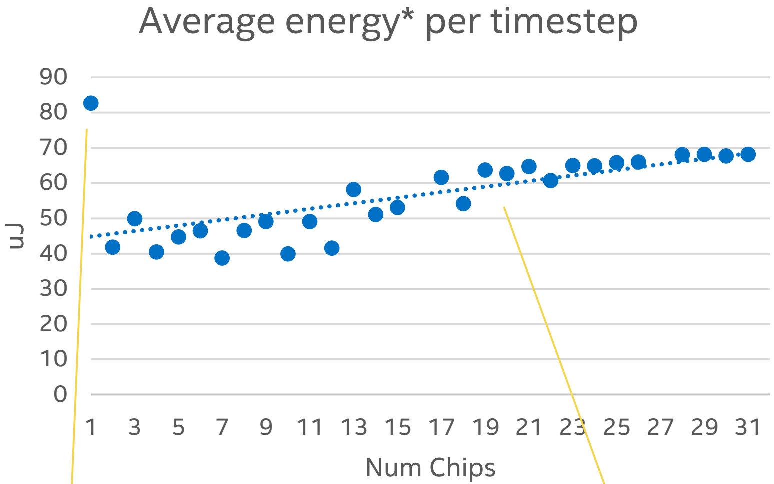
Distributing the 50x50x50 lattice over Nahuku



Search performance improves from 1 to 7 chips, degrading thereafter as chip-to-chip synchronization and spike communication overhead dominate.

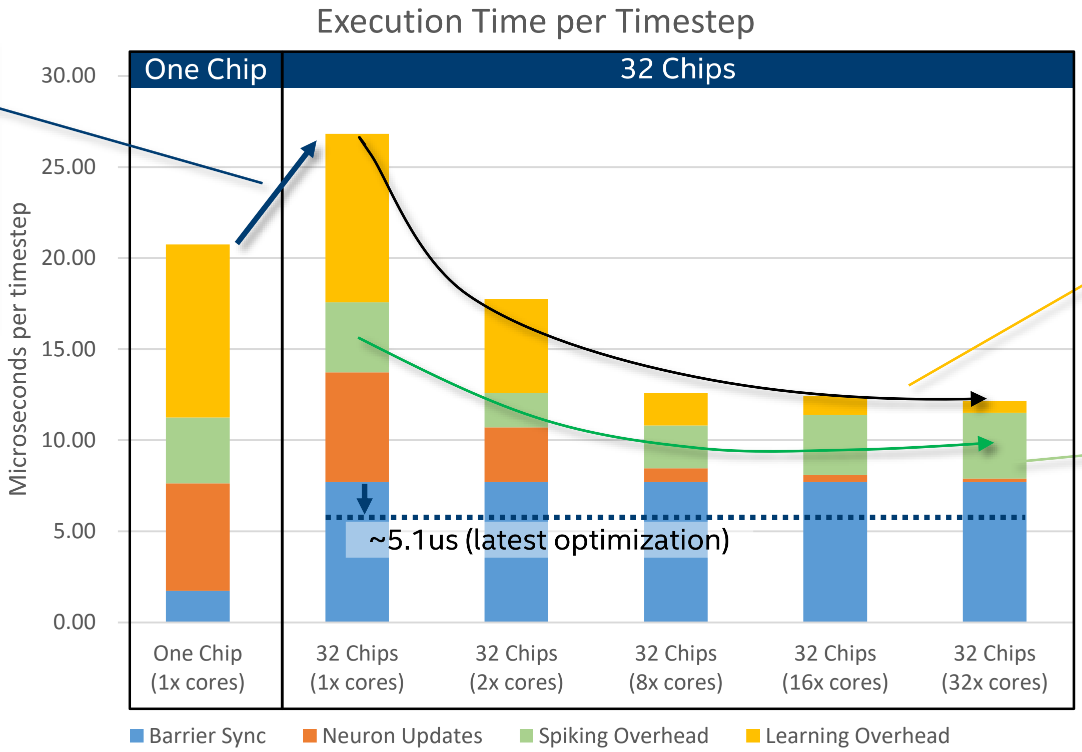


Single chip case has *worst* energy efficiency due to leakage

Energy efficiency degrades with increasing parallelism due to increasing chip-to-chip communication cost

*Includes energy due to board-level leakage/idle power

Increasing **core parallelism** with **fixed chip count**



Fixed 128-way core parallelism. Slowdown due to **increased barrier sync time** over 32 chips vs 1 chip

Learning overhead **decreases** with increasing core parallelism

Spike overhead decreases, then **increases** with increasing core parallelism