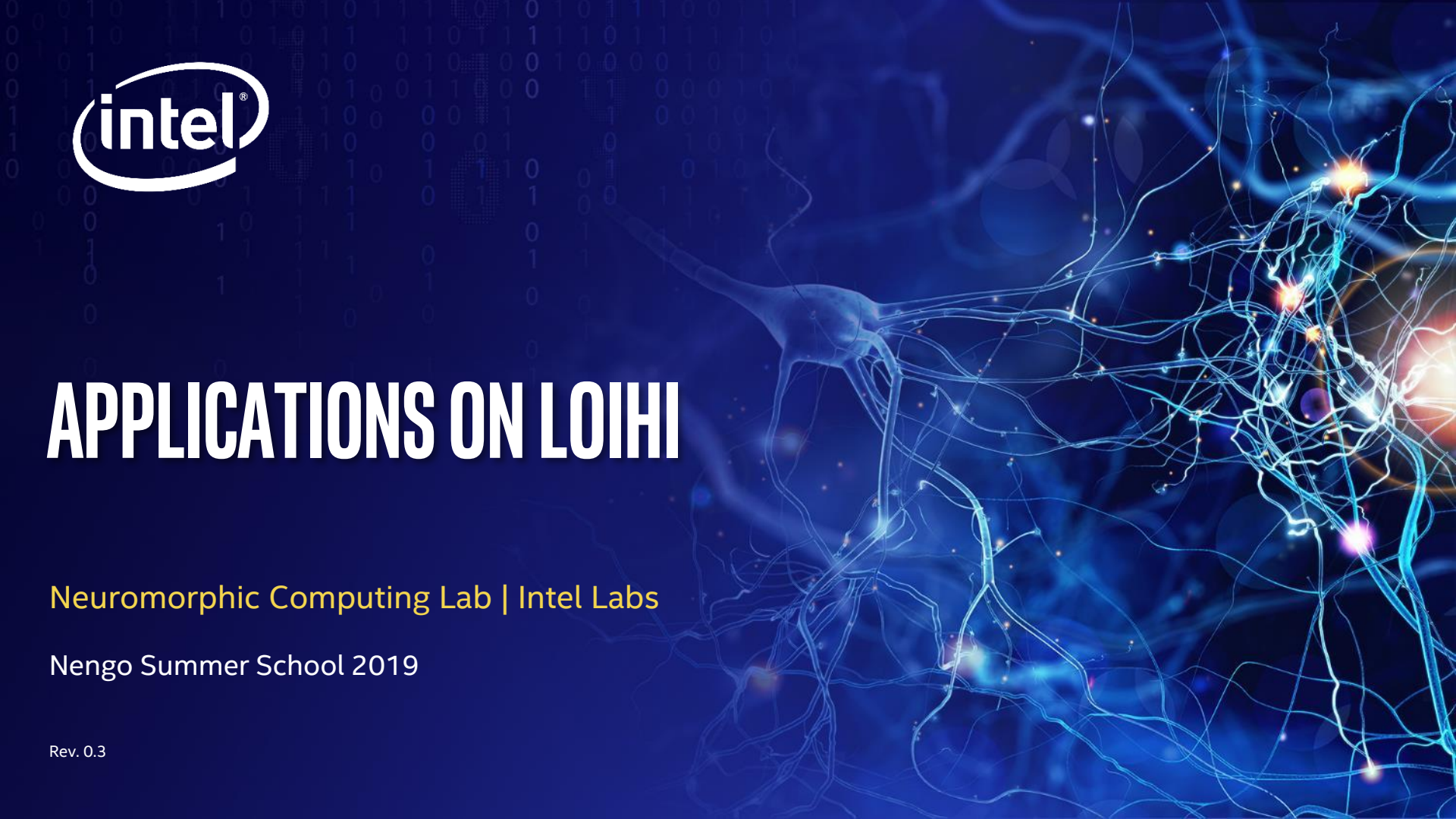


APPLICATIONS ON LOIHI

Neuromorphic Computing Lab | Intel Labs

Nengo Summer School 2019

Rev. 0.3

LEGAL INFORMATION

This presentation contains the general insights and opinions of Intel Corporation ("Intel"). The information in this presentation is provided for information only and is not to be relied upon for any other purpose than educational. Intel makes no representations or warranties regarding the accuracy or completeness of the information in this presentation. Intel accepts no duty to update this presentation based on more current information. Intel is not liable for any damages, direct or indirect, consequential or otherwise, that may arise, directly or indirectly, from the use or misuse of the information in this presentation.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer.

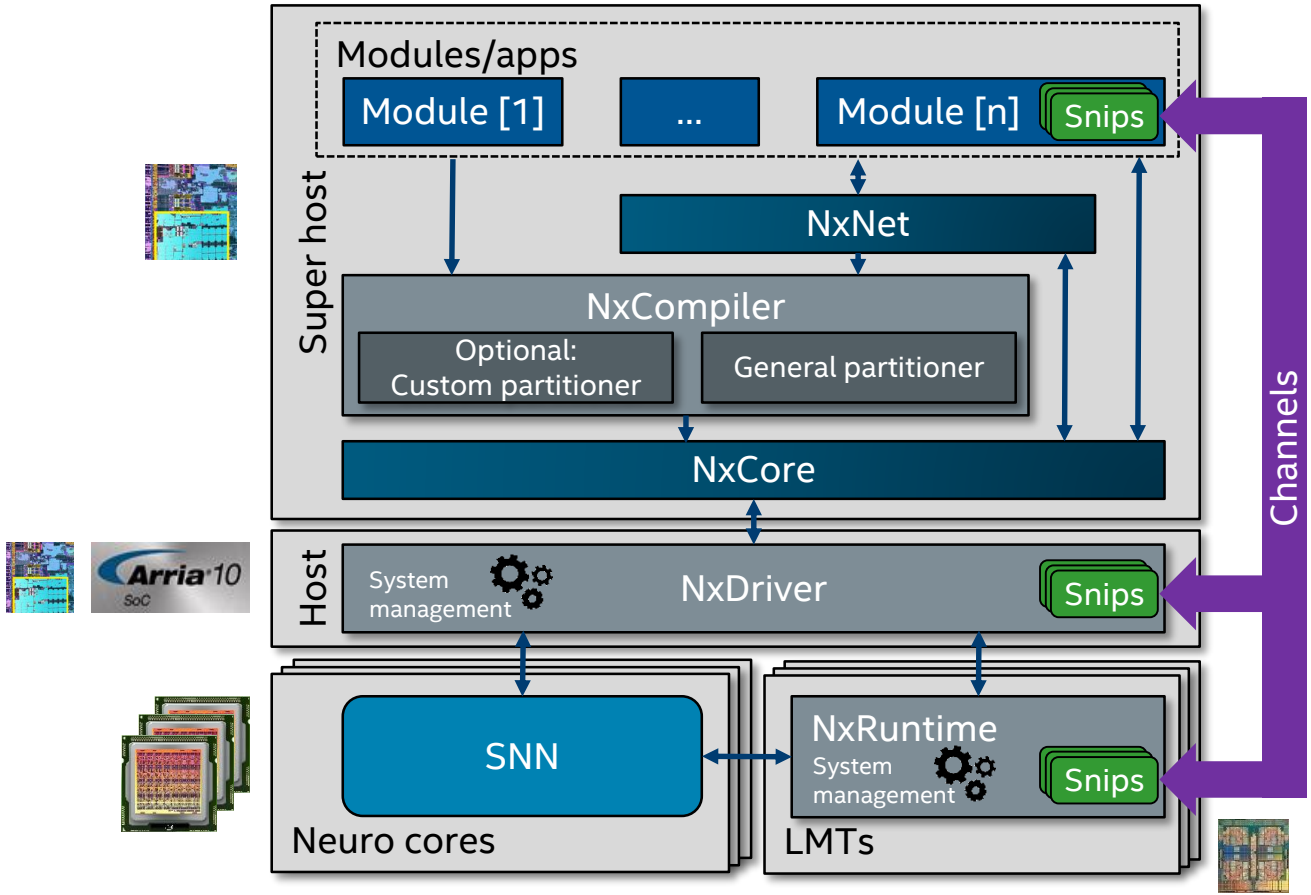
No computer system can be absolutely secure. No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document. Intel, the Intel logo, Movidius, Core, and Xeon are trademarks of Intel Corporation in the United States and other countries.

*Other names and brands may be claimed as the property of others

Applications on Loihi

- SW Stack Components
- Example Applications

SW stack execution on heterogeneous HW



Applications on Loihi

- SW Stack Components
- Example Applications
  - DVS
  - Path Planning
  - Olfactory Neural Circuit
  - Constraint Satisfaction Problems
  - LASSO with LCA
  - Time and Energy Probes

DVS WITH LOIHI

Neuromorphic Computing Lab | Intel Labs

Nengo Summer School 2019

LEGAL INFORMATION

This presentation contains the general insights and opinions of Intel Corporation ("Intel"). The information in this presentation is provided for information only and is not to be relied upon for any other purpose than educational. Intel makes no representations or warranties regarding the accuracy or completeness of the information in this presentation. Intel accepts no duty to update this presentation based on more current information. Intel is not liable for any damages, direct or indirect, consequential or otherwise, that may arise, directly or indirectly, from the use or misuse of the information in this presentation.

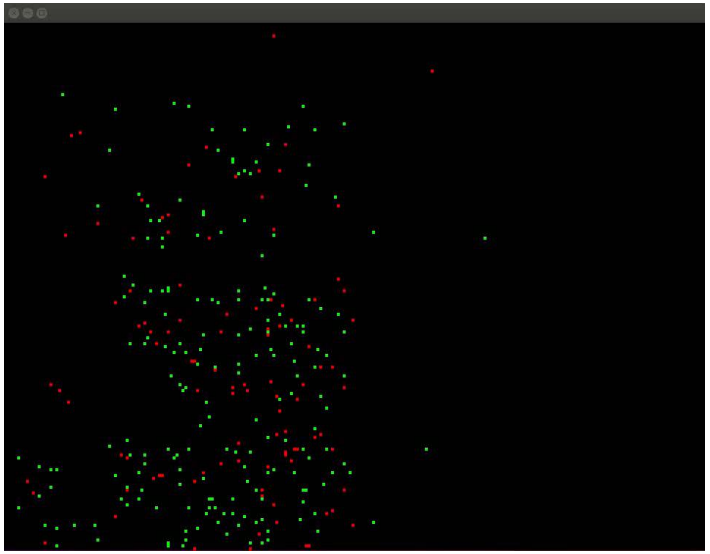
Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer.

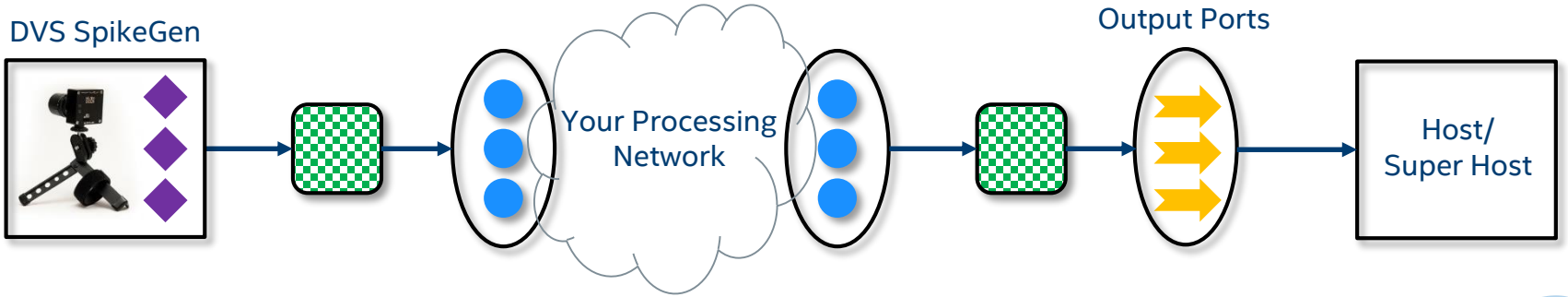
No computer system can be absolutely secure. No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document. Intel, the Intel logo, Movidius, Core, and Xeon are trademarks of Intel Corporation in the United States and other countries.

*Other names and brands may be claimed as the property of others

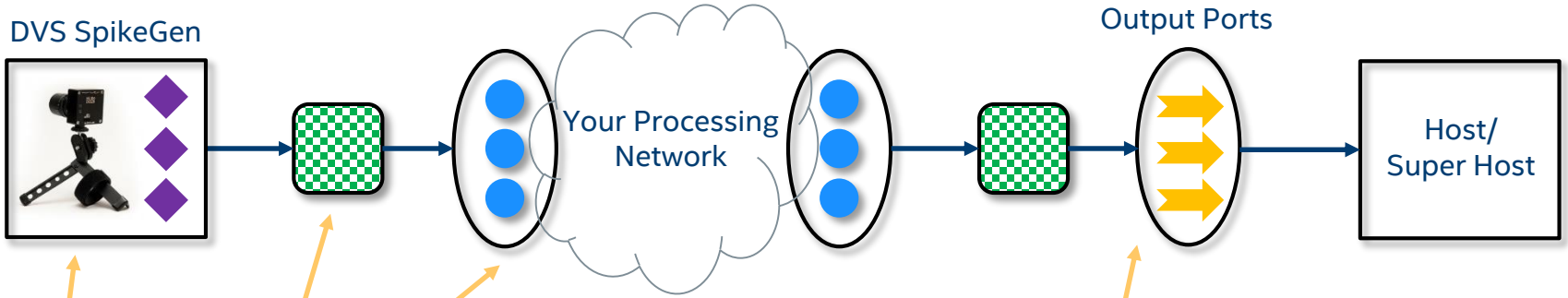
DVS


ubuntu
16.04.5 LTS
Kapoho Bay




DVS SpikeGen
Your Processing Network
Output Ports
Host/ Super Host

DVS

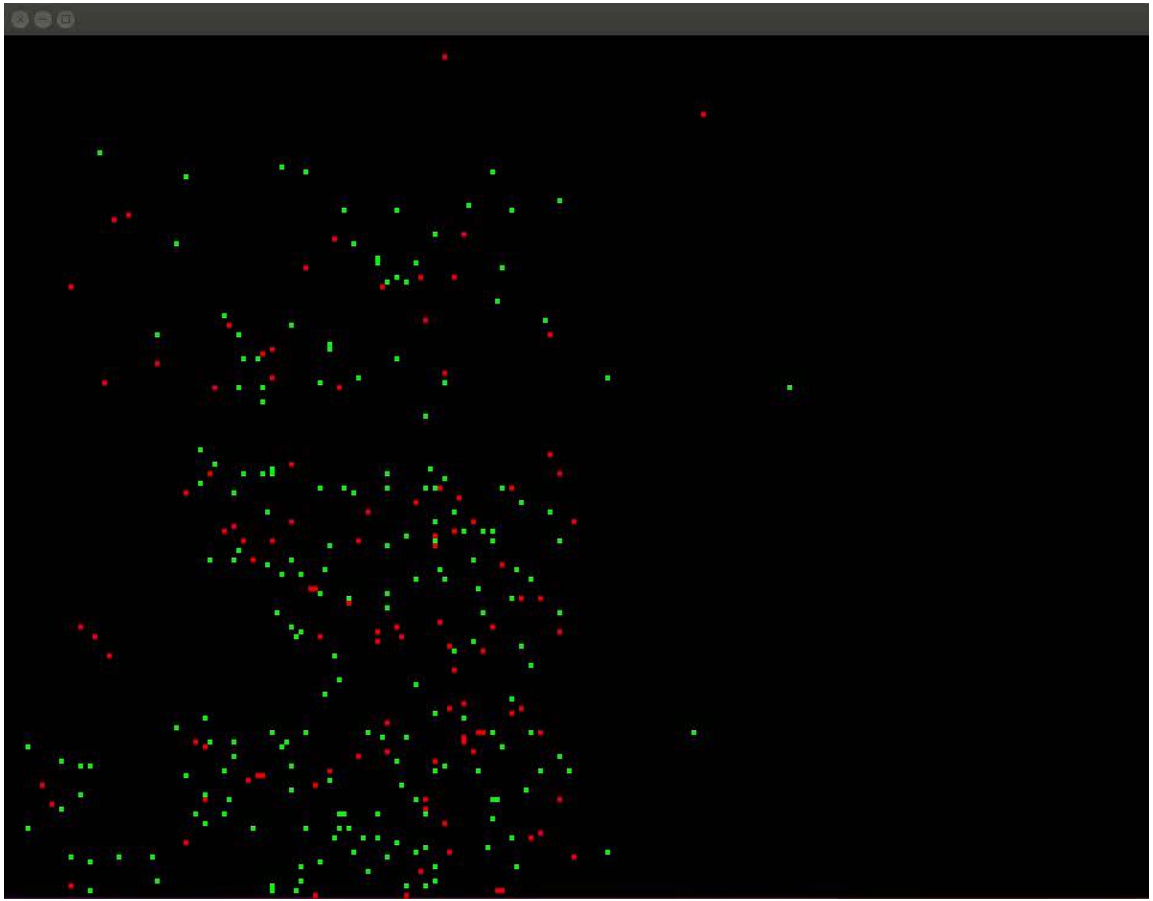


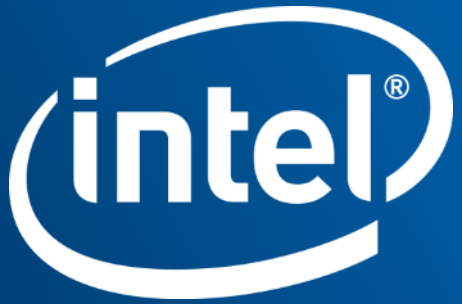

```
# Create a compartment group
cg1 = net.createCompartmentGroup(size=dvsSpikeGen.numPorts,
                                 prototype=cp)

# Create a connection prototype
connproto = nx.ConnectionPrototype(weight=255,
                                   signMode=nx.SYNAPSE_SIGN_MODE.EXCITATORY)

# Create connection mask to have 1:1 mapping between pixels and compartments
cMask = identity(dvsSpikeGen.numPorts)
connGrp1 = dvsSpikeGen.connect(cg1, prototype=connproto,
                               connectionMask=cMask)
```

```
# Create a DVS spike gen process
dvsSpikeGen = net.createDVSSpikeGenProcess(xPixel=240, yPixel=180,
                                           polarity=2)
```

```
# Create spike output port group and make 1:1 connection to compartments
outPortGrp = net.createSpikeOutputPortGroup(size=dvsSpikeGen.numPorts)
connGrp2 = cg1.connect(outPortGrp, connectionMask=cMask)
```

DVS





Questions?